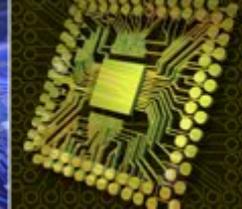
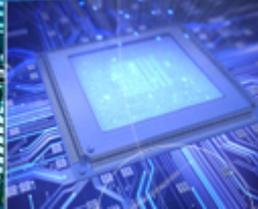
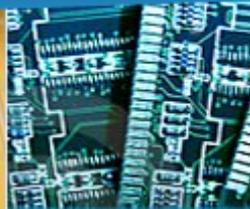
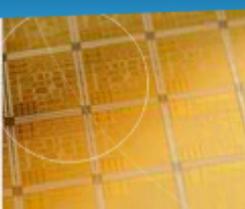


Silicon Turnkey Solutions

Burn-in capabilities



• Why Changes to Burn In

- Next Gen Processing
- High complexity
- Reduced voltage
- Feature size
- Power dissipation
- Multi functional blocks

Silicon Turnkey Solutions Early Burn-in capabilities

▪ Conventional chamber based Burn-in & test system

- ✓ Enhanced performance with STS methodology- backplane
- ✓ Overcome Improper temperature control
- ✓ Eliminate Noise from fans and power supplies, glitches
- ✓ GOOBI, conclusion BI causes more damage without regulation of DUT
- ✓ Slew Rate Management

Conventional Chamber Based Burn-in System

Burn In Equipment

- High noise/glitch suppression mechanism for power supplies, oven and utilities
- Precision Power Supplies
- Solid State Relays
- Output Monitoring
- Deep Test Pattern Depth
- High fault coverage using 128 independent I/O channels + 16 Hi-Z
- Minimal Interruption; Direct failure correlation



Ovens (Isuzu-Soyokaze, Hastest, EDA, AEHR-PBC4)

- Customized for 4 – 6 boards maximum
- Customized air flow
- Low noise, no glitch, no contactors

Un-interrupted ovens for Life tests



CONVENTIONAL BURN-IN BOARDS

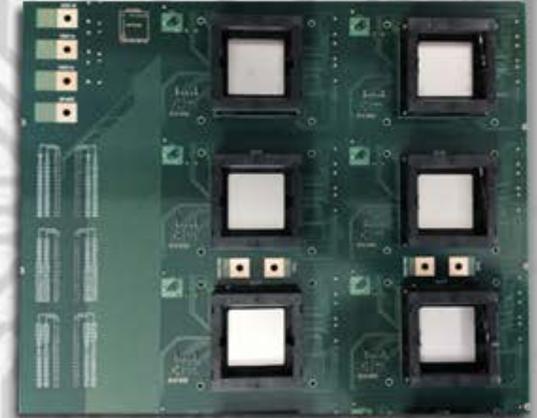
Design

Impedance Control: 15 to 100 OHMS

Resistance, capacitance and delay control

Trace width consideration (up to 3 Mil)

Differential pair routing with skew tuning



Maintenance

Frequent real-time check of all sockets and components

Specifications

Four to five power supplies maximum per board

40 Amps maximum per board

Boards rated up to 150C



CONVENTIONAL BURN-IN BOARDS continued

Vector Depth

128 driven channels

16 Bits or Tri-state availability

Up to 32 M Bit depth for each pin

20 MHz and 32 MHz free running clocks

Driver capable of 10 MHz Master clock



Conventional Power Supplies

- Solid State Power Supplies With GPIB Control
- Ultra-high Full Scale Accuracy
- Minimum Noise and Ripple
- Ultra Accurate Regulation



STS Burn-in Next Generation capabilities

▪MCC chamber based Burn-in & test system

- ✓Sophisticated and expensive burn-in system
- ✓Hardware investment
- ✓Capital equipment investment

MCC chamber based Burn-in & test system

High power burn-in system (HPB-5B)

Specification

Digital I/O Channels	128
Programmable voltage regulators	11
Max current	800A per board
Continuous heat sink temp monitor	Yes
Continuous junction temp monitor	Yes
Power supply regulation	Yes
Continuous voltage monitor	Yes
Max positions per board	24
Max power	150W

Limitations of MCC chambers based Burn-in & test system

- System power supply instabilities
- On-board parallel power - DUT to DUT variations
- Device thermal management – board level only
- Device to board contact integrity challenges
- Limitation at dynamic functional exercise
- Long lead-times for high temperature hardware
- Inability to monitoring high speed signals in situ
- Capacity constraints - limited scalability
- Fixed MEGA chamber – ergonomically unfriendly

STS Third Generation capabilities

▪ Burn-in & test system still needed improvement: Fresh Look

- ✓ Concept change from heating DUT to managing the DUT

- ✓ Force cool to get acceleration

- ✓ 45nm DUT already at 125C, Historic DUT 55C use condition

- ✓ Challenge:

 - ✓ How to bring output monitoring to BI

 - ✓ Guaranteed exercise and NOT overstressing

 - ✓ Historically 10K transistors, now packages have 5-10B transistors

 - ✓ I billion combinations on the chip, evaluate weakest link

 - ✓ How to bring high power, low voltage, high frequency, massive level of

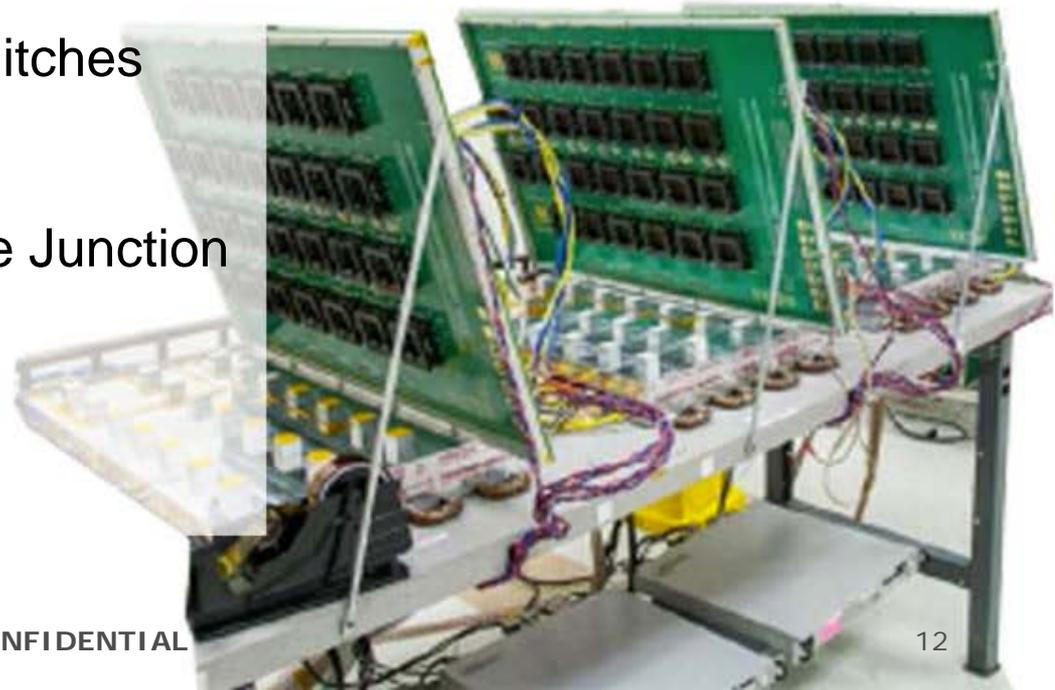
 - functional blocks into BI

 - ✓ Fault grading on the chip

Innovative Thermal Controller 360 (ITC360) based Burn-in system

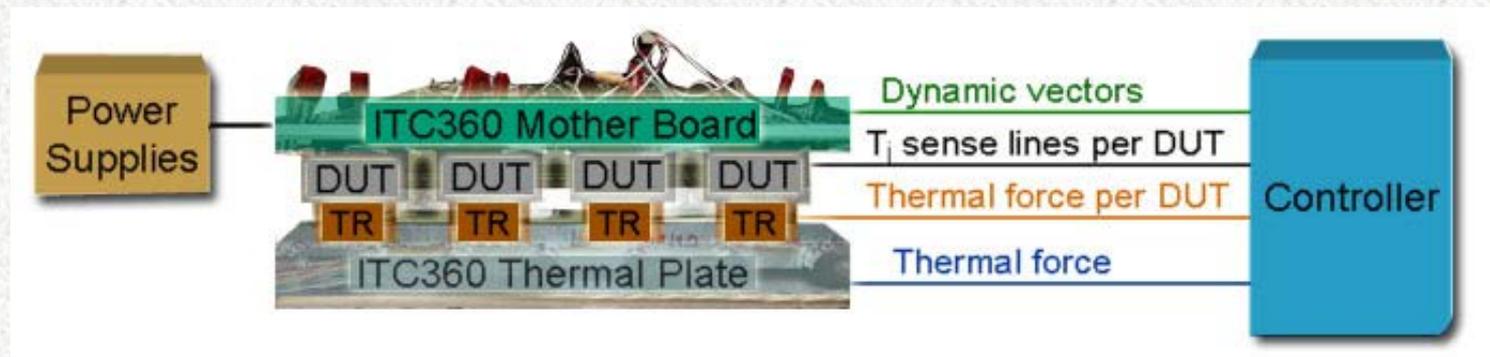
Salient Features

- Bench based dynamic thermo electric Cooling and Heating for each DUT
- Rapid response thermal management, real time to each DUT
- No barriers dynamic exercise, Speed, Vector depth and loops
- Standard Commercial burn-in Sockets
- Eliminate Noise and inductive glitches
- High speed signals to the DUT
- Regulate Case, Ambient and the Junction



Active Monitoring and Thermal Regulation

- Conductive thermal regulation
 - Provides accurate regulation & quick response time
- Thermal Plate provides stable board temperature
- Each DUT junction temperature (T_j) is regulated
 - T_j sensed thru thermal diode on device
 - T_j heated or cooled via Thermal Regulator (TR)
 - T_j controlled to $\pm 1^\circ\text{C}$



ITC360 Features & Benefits

- **Burn-in at rated voltages & speed**
 - ✓ No need to lower power or reduce frequencies
- **Open-air implementation**
 - ✓ Enables significantly lower hardware costs
 - ✓ Facilitates real-time in situ monitoring access
- **Full dynamic burn-in capability**
 - ✓ Via National Instruments hardware
- **Implementation flexibility for unique requirements**
 - ✓ Not constrained by physical chamber
- **Modular design**
 - ✓ Expandable for greater capacity or future needs
 - ✓ Reduced carbon footprint (less power, smaller, etc.)

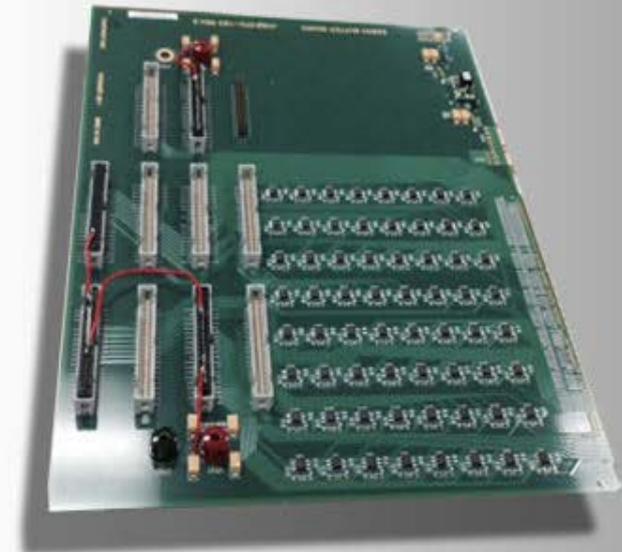
Drivers & Pattern Depth

Drivers

- Custom STS drivers
- Designed to accommodate burn-in conditions with:
 - Low voltage, High Current , High Frequency
- Monolithic driver (buffer) circuitry with tri-state capability (Elantec-EI-7156)
- 15nSec switching rise and fall times
- 0.5nSec rise/fall time driver to driver mismatch
- Designed for 1.0 to 3.3V Vih BI applications
- 50mA Channel per driver

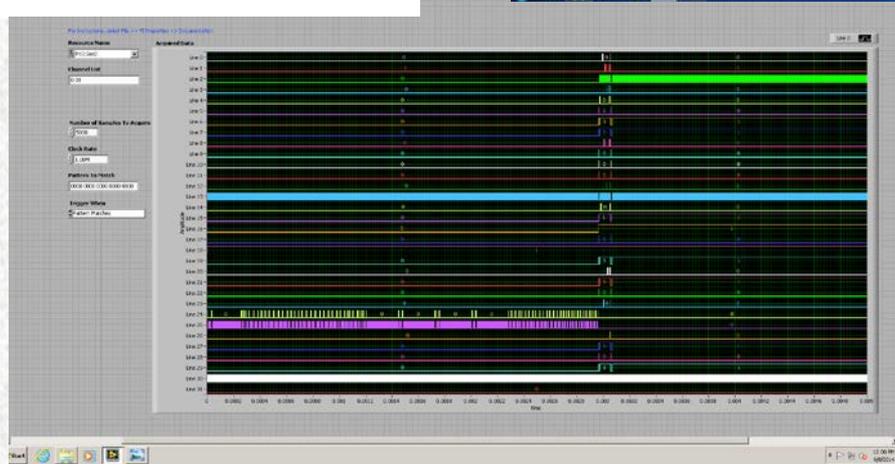
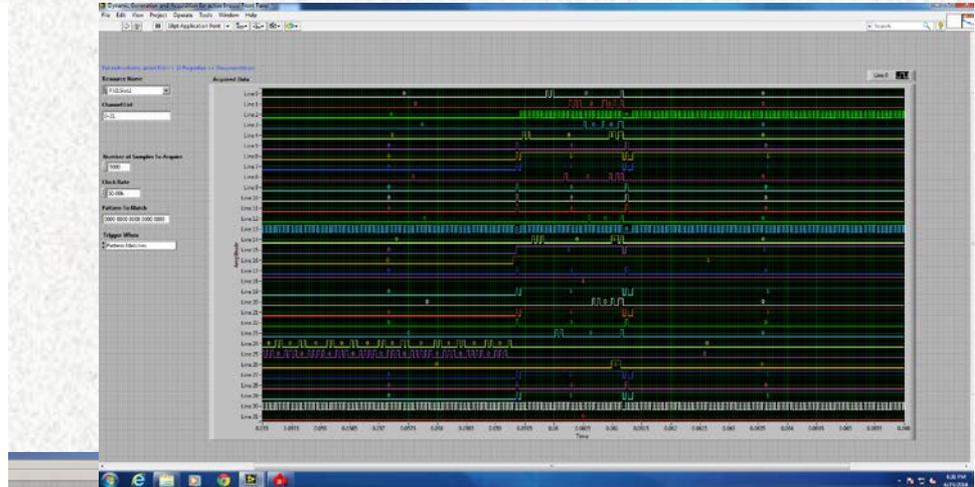
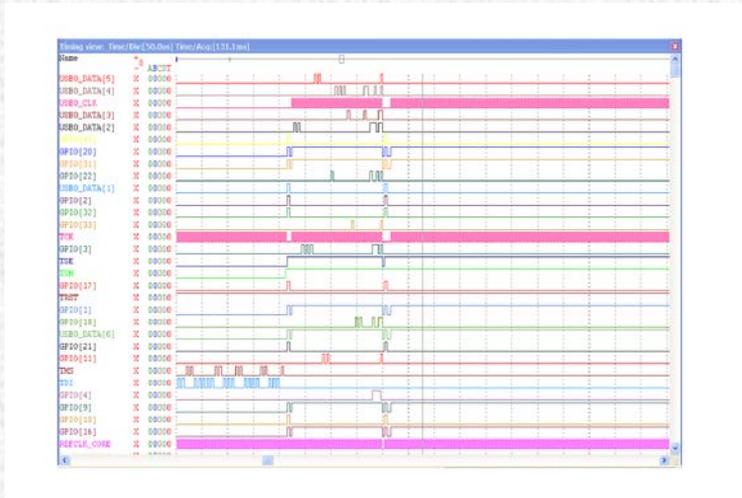
Pattern Depth

- 16M vector depth across 128 channels + 16 Hi-z
- 32M vector depth across 96 channels + 8 Hi-z



NATIONAL INSTRUMENTMENTS – AWG Arbitrary Waveform Generator

Used to generate vector stimulus and frequency input stimulus to the DUT.

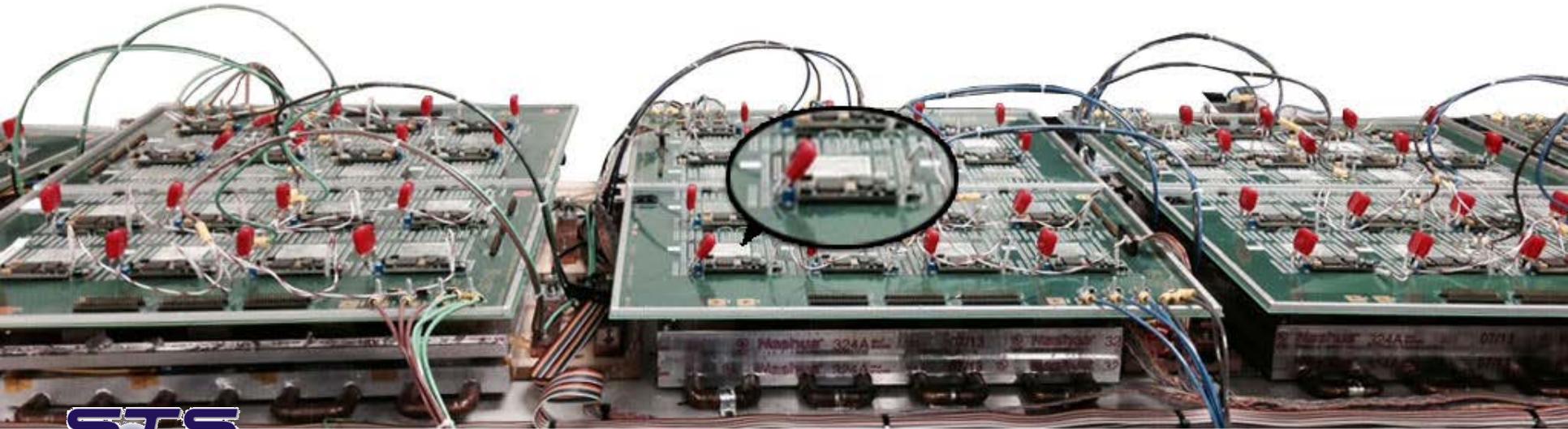


Significant Benefits

- Valuable Level II (board level) reliability data
- Wide array of instrumentation
 - ✓ Application specific depending on stress requirements
- Direct probe access for high speed instruments
- Full design flexibility & scalability up to boards
- Significant cost savings
 - ✓ Standard sockets, cables and connectors
- Faster time-to-market
 - ✓ Standard component lead times

ITC360 Value Proposition

- Full dynamic burn-in capability
- Regulated accurate burn-in conditions
- Significant overall cost savings (~50%)
- Valuable development time savings (~6 weeks)
- Flexibility & accessibility



ITC360 Value Proposition continued

- Bringing Intelligence to Burn In
- Post BI analysis
- Pre and Post Delta Computation
- Device level thermal footprint change
- Extensive high frequency, dynamic exercise of the chip
- Stimulus generation
- P/S control at DUT, not to the BI board
- Validity of BI is looking for signal change at ATE
- Not Go/No GO
- Peak performance, timing peak power. **Full Throttle** changes

Prepared exclusively for

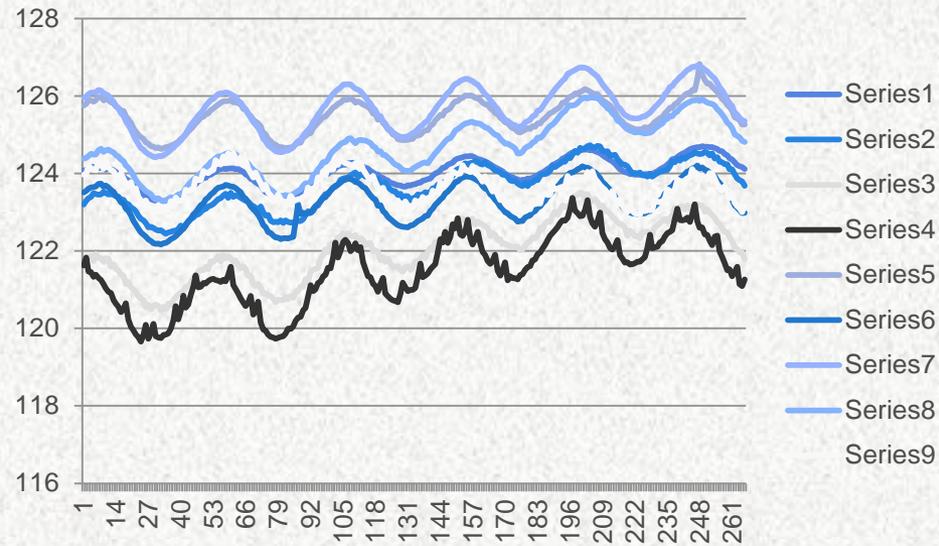


Temperature Sensing Diode Calibration

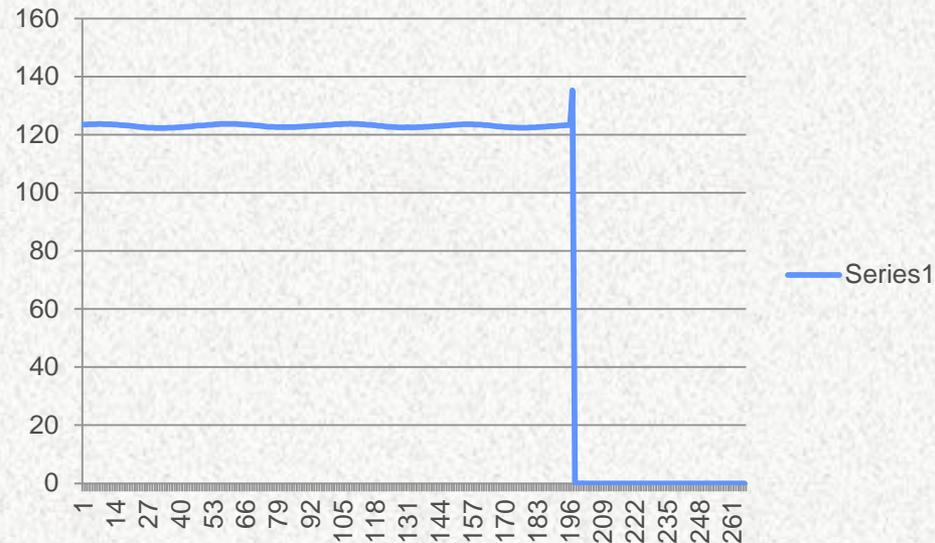
Device	TILERA GX72 1847L
Package	FCBGA
Customer	Tilera Corporation

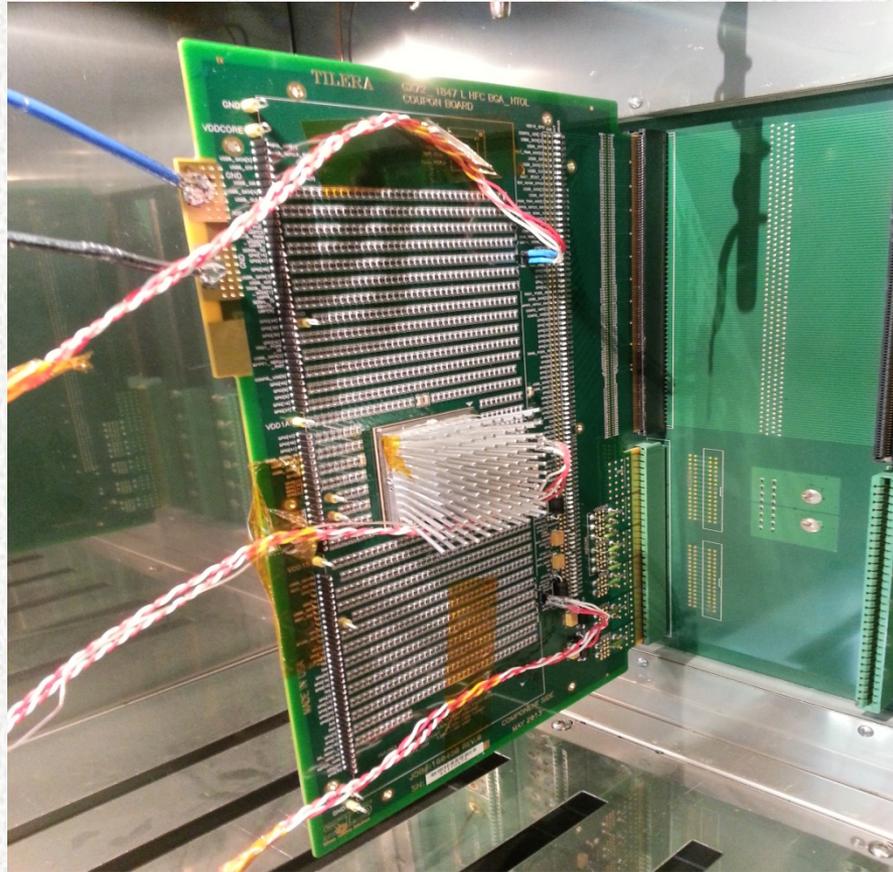


Real Time Ti Monitor and regulation



Real Time Capture of a 'Thermal Runaway'





ITC360 and HPB-5 Comparison Specifications & Capabilities

	ICT360	HPB-5B	Comments
Max number of DUTs	Unlimited	384	
Max power per DUT	250> Watts	150 Watts	
Max current per board	1,000> Amps	800 Amps	
T _j regulation	125°C (+/- 1°C)	125°C	
Regulated power	Yes (Each DUT)	NO	ITC360 offer Rapid Heating & Cooling of each DUT independently
Heating & Cooling per DUT	Yes	NO	ITC360 Monitors the Temperature of each device independently
Direct DUT signal access	Yes	NO	ITC360 Monitors the Signal access of each device independently
Digital I/O Channels per board	128	128	
Max vector pattern depth	64M per channel	8M per channel	
Infinite vector looping	Yes	Yes	
High-speed differentials	Yes	Yes	
RF inputs	Yes	NO	
Socketless board option	Yes	N/A	
On-the-fly timing sets	Yes (unlimited)	8	
Digital Frequency	550 MHz	10Mhz	ITC360: AT speed available
System-level protocol option	Yes via NI hardware	NO	

The
United
States
of
America



The Director of the United States
Patent and Trademark Office

Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

Therefore, this

United States Patent

Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America, and if the invention is a process, of the right to exclude others from using, offering for sale or selling throughout the United States of America, or importing into the United States of America, products made by that process, for the term set forth in 35 U.S.C. 154(a)(2) or (c)(1), subject to the payment of maintenance fees as provided by 35 U.S.C. 41(b). See the Maintenance Fee Notice on the inside of the cover.

Michelle K. Lee

Deputy Director of the United States Patent and Trademark Office



US008766656B2

(12) **United States Patent**
Malik et al.

(10) **Patent No.:** US 8,766,656 B2
(45) **Date of Patent:** Jul. 1, 2014

(54) **SYSTEMS AND METHODS FOR THERMAL CONTROL**
(71) Applicants: Zafar Malik, Milpitas, CA (US); David Jackson, Milpitas, CA (US)
(72) Inventors: Zafar Malik, Milpitas, CA (US); David Jackson, Milpitas, CA (US)
(73) Assignee: Silicon Turnkey Solutions Inc., Milpitas, CA (US)
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(58) **Field of Classification Search**
None
See application file for complete search history.

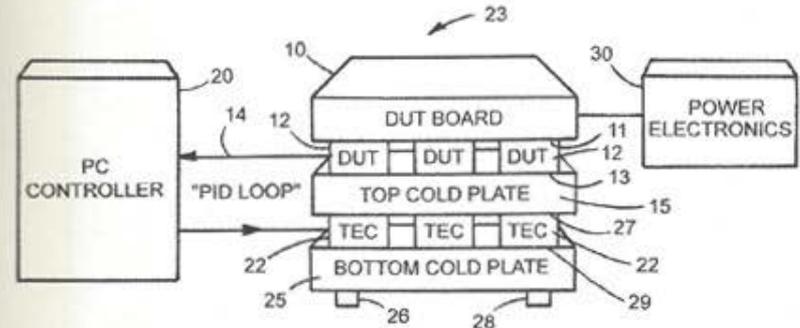
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* cited by examiner

(21) Appl. No.: 13865,005
(22) Filed: Apr. 17, 2013
(74) Attorney, Agent, or Firm — Ellahie & Ferooqi LLP

(65) **Prior Publication Data**
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Related U.S. Application Data
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(51) **Int. Cl.**
G01R 31/10 (2006.01)
G01R 31/28 (2006.01)
(52) **U.S. Cl.**
CPC G01R 31/2875 (2013.01); G01R 31/2877 (2013.01)
USPC 324/750.05; 324/750.11; 324/750.14

(57) **ABSTRACT**
The present invention relates generally to a system and a method for thermal control. More particularly, the invention encompasses an apparatus for thermal control and management of at least one device under test (DUT). The inventive thermal control and management apparatus also allows for the management of a plurality of devices under test, and with each device under test having its own testing regimen. The thermal control and management of the device under test (DUT) is managed using at least one thermoelectric element or cooler (TEC), which can be used to either heat or cool the corresponding device under test (DUT).

23 Claims, 6 Drawing Sheets





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